What is claimed is :

1. A circuit for controlling a cache system having a store queue having plural stages for storing store instructions, said circuit including :

a first comparator circuit for comparing, in view of index and off-set, an instruction with tag-retrieval to said store instructions stored in said store queue ; and

a stalling circuit for selectively stalling said instruction with tag-retrieval if said instruction with tag-retrieval corresponds, in view of not only index but also off-set, to at least one of said store instructions.

2. The circuit as claimed in claim 1, wherein said stalling circuit does not stall said instruction with tag-retrieval if said instruction with tag-retrieval corresponds, in view of index, to at least one of said store instructions but does not correspond, in view of off-set, to at least one of said store instructions

3. The circuit as claimed in claim 1, wherein said stalling circuit does not stall said instruction with tag-retrieval if a subsequent instruction with tag-retrieval to said instruction with tag-retrieval corresponds, in view of index, to at least one of said store instructions.

4. The circuit as claimed in claim 1, further comprising :

a second comparator circuit for comparing, in view of index and

way, said instruction with tag-retrieval to said store instructions stored in said store qucue ;

a executing unit for executing said store instructions in said store queue ; and

a replacing unit for replacing two instructions in order, and

wherein said stalling circuit does not stall said instruction with tag-retrieval if a subsequent instruction with tag-retrieval to said instruction with tag-retrieval corresponds, in view of index, to at least one of said store instructions, and

wherein if said instruction with tag-retrieval has a cache-miss and if said instruction with tag-retrieval corresponds, in view of index and way, to at least one of said store instructions, then said executing unit executes said store instructions in said store queue prior to replace process by said replacing unit.

5. The circuit as claimed in claim 4, wherein if a subsequent instruction with tag-retrieval to said instruction with tag-retrieval corresponds, in view of index and off-set, to said store instruction, then said stalling circuit stalls said instruction with tag-retrieval.

6. The circuit as claimed in claim 5, wherein said subsequent instruction with tag-retrieval is a load instruction.

7. The circuit as claimed in claim 4, wherein if said instruction with

tag-retrieval is a store instruction and has a cache-miss and if said instruction with tag-retrieval corresponds, in view of index and way, to at least one of said store instructions, then said executing unit executes said store instructions in said store queue prior to storing said instruction with tag-retrieval into said store queue.

8. The second comparator circuit as claimed in claim 4, wherein said first comparator circuit comprises an index match detecting unit, and said second comparator circuit comprises a store queue hit detecting unit.

9. The circuit as claimed in claim 1, wherein said cache system has a data cache structure including plural ways.

10. A circuit for controlling a cache system having a store queue having plural stages for storing store instructions, said circuit including :

a first comparator circuit for comparing, in view of index and off-set, a subsequent instruction with tag-retrieval, which is not of store instruction, to said store instructions stored in said store queue ; and

a stalling circuit for selectively stalling said instruction with tag-retrieval if said subsequent instruction with tag-retrieval corresponds, in view of not only index but also off-set, to at least one of said store instructions.

11. A circuit for controlling a cache system having a store queue

having plural stages for storing store instructions, said circuit including :

a first comparator circuit for comparing, in view of index and off-set, a subsequent instruction with tag-retrieval, which is not ~~of~~ a store instruction, to said store instructions stored in said store queue ;

a second comparator circuit for comparing, in view of index and way, said subsequent instruction with tag-retrieval to said store instructions stored in said store queue ; and

a stalling circuit for selectively stalling said subsequent instruction with tag-retrieval if said instruction with tag-retrieval corresponds, in view of at least one set of a first set of index and off-set and a second set of index and way, to at least one of said store instructions.

12. A method for controlling a cache system having a store queue having plural stages for storing store instructions, said method including :

comparing, in view of index and off-set, an instruction with tag-retrieval to said store instructions stored in said store queue ; and

selectively stalling said instruction with tag-retrieval if said instruction with tag-retrieval corresponds, in view of not only index but also off-set, to at least one of said store instructions.

13. The method as claimed in claim 12, wherein said instruction with tag-retrieval is not stalled if said instruction with tag-retrieval corresponds, in view of index, to at least one of said store instructions but does not correspond, in view of off-set, to at least one of said store

instructions

14. The method as claimed in claim 12, wherein said instruction with tag-retrieval is not stalled if a subsequent instruction with tag-retrieval to said instruction with tag-retrieval corresponds, in view of index, to at least one of said store instructions.

15. The method as claimed in claim 12, further comprising :

comparing, in view of index and way, said instruction with tag-retrieval to said store instructions stored in said store queue ;

executing said store instructions in said store queue ; and

replacing two instructions in order, and

wherein said instruction with tag-retrieval is not stalled if a subsequent instruction with tag-retrieval to said instruction with tag-retrieval corresponds, in view of index, to at least one of said store instructions, and

wherein if said instruction with tag-retrieval has a cache-miss and if said instruction with tag-retrieval corresponds, in view of index and way, to at least one of said store instructions, then said store instructions in said store queue are executed prior to replace process by said replacing unit.

16. The method as claimed in claim 15, wherein if a subsequent instruction with tag-retrieval to said instruction with tag-retrieval corresponds, in view of index and off-set, to said store instruction, then said

instruction with tag-retrieval is stalled.

17. The method as claimed in claim 16, wherein said subsequent instruction with tag-retrieval is a load instruction.

18. The method as claimed in claim 15, wherein if said instruction with tag-retrieval is a store instruction and has a cache-miss and if said instruction with tag-retrieval corresponds, in view of index and way, to at least one of said store instructions, then said store instructions in said store queue are executed prior to storing said instruction with tag-retrieval into said store queue.

19. The method as claimed in claim 12, wherein said cache system has a data cache structure including plural ways.

20. A method for controlling a cache system having a store queue having plural stages for storing store instructions, said method including :

comparing, in view of index and off-set, a subsequent instruction with tag-retrieval, which is not of a store instruction, to said store instructions stored in said store queue ; and

selectively stalling said instruction with tag-retrieval if said subsequent instruction with tag-retrieval corresponds, in view of not only index but also off-set, to at least one of said store instructions.

21. A method for controlling a cache system having a store queue having plural stages for storing store instructions, said method including :

comparing, in view of index and off-set, a subsequent instruction with tag-retrieval, which is not of store instruction, to said store instructions stored in said store queue ;

further comparing, in view of index and way, said subsequent instruction with tag-retrieval to said store instructions stored in said store queue ; and

selectively stalling said subsequent instruction with tag-retrieval if said instruction with tag-retrieval corresponds, in view of at least one set of a first set of index and off-set and a second set of index and way, to at least one of said store instructions.